ABSTRACT

A nonconductive hydrogen barrier layer is deposited on a substrate and completely covers the surface area over a memory capacitor and a MOSFET switch of an integrated circuit memory cell. A portion of an insulator layer adjacent to the bottom electrode of a memory capacitor is removed by etching to form a moat region. A nonconductive oxygen barrier layer is deposited to cover the sidewall and bottom of the moat. The nonconductive oxygen barrier layer and a conductive diffusion barrier beneath the capacitor together provide a substantially continuous diffusion barrier between the capacitor and a switch. Also, the nonconductive hydrogen barrier layer, the nonconductive oxygen barrier, and the conductive diffusion barrier substantially completely envelop the capacitor, in particular a ferroelectric thin film in the capacitor.